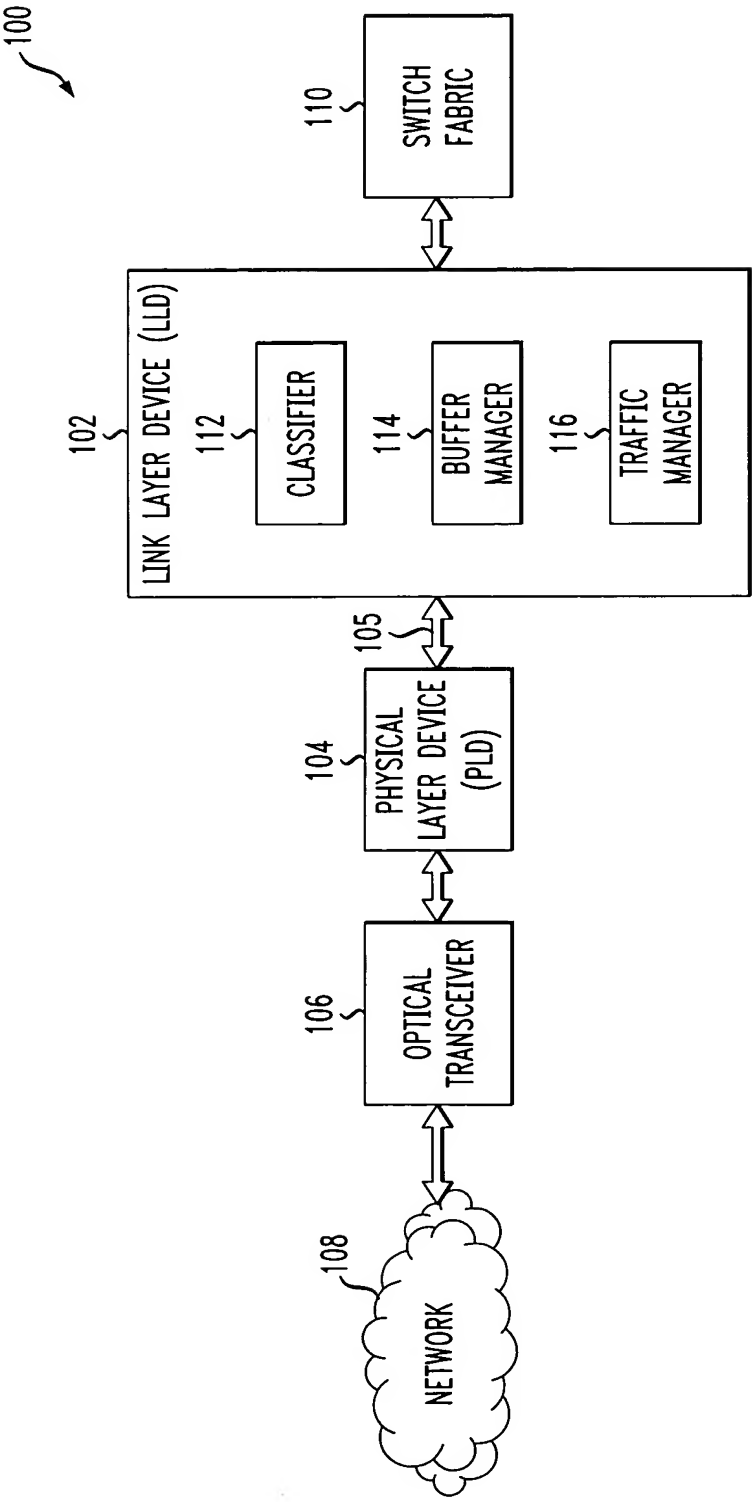


FIG. 1

FIG. 2

FIELD NAME	SIZE (BITS)
FLAG FIELD (F)	8 BITS
ADDRESS FIELD (A)	8 BITS
CONTROL FIELD (C)	8 OR 16 BITS
INFORMATION FIELD (I)	VARIABLE
FRAME CHECK SEQUENCE (FCS)	16 OR 32 BITS

FIG. 3

	PACKET OVERHEAD (ASSUMING MAX SIZE FOH = 8B)			
	FOH	SOH	PS	% OH
NO STUFFING, MIN SIZED PACKET	8	0	40	20%
MAX STUFFING, MIN SIZED PACKET	8	8	40	40%
NO STUFFING, MAX SIZED PACKET	8	0	9600	0.08%
MAX STUFFING, MAX SIZED PACKET	8	1920	9600	20%

ASSUMPTIONS:

a) PACKET SIZE (PS):
40 - 9600 BYTES

b) WORST-CASE HDLC BIT STUFFING OVERHEAD (SOH)
20% OF (a) = 8 - 1920 BYTES

c) HDLC FRAME OVERHEAD (FOH)
5 - 8 BYTES

FIG. 4

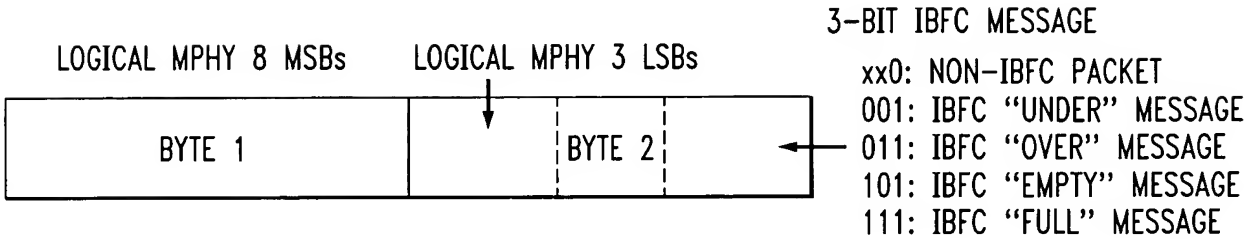
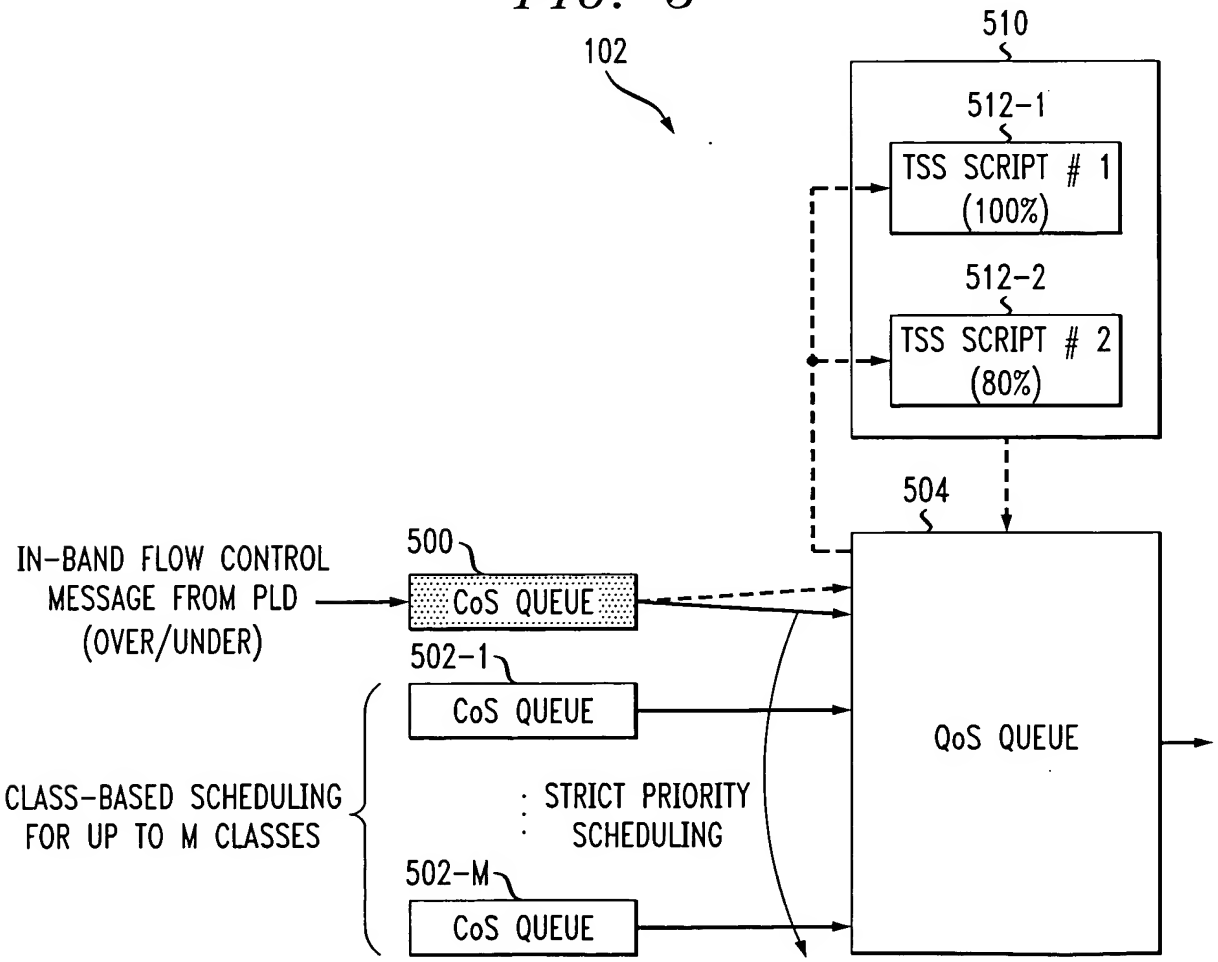

LOGICAL MPHY 8 MSBs
LOGICAL MPHY 3 LSBs
BYTE 1
BYTE 2
3-BIT IBFC MESSAGE
xx0: NON-IBFC PACKET
001: IBFC "UNDER" MESSAGE
011: IBFC "OVER" MESSAGE
101: IBFC "EMPTY" MESSAGE
111: IBFC "FULL" MESSAGE

FIG. 5


102
510
512-1
TSS SCRIPT # 1
(100%)
512-2
TSS SCRIPT # 2
(80%)
504
500
IN-BAND FLOW CONTROL
MESSAGE FROM PLD
(OVER/UNDER)
CoS QUEUE
502-1
CoS QUEUE
CLASS-BASED SCHEDULING
FOR UP TO M CLASSES
STRICT PRIORITY
SCHEDULING
502-M
CoS QUEUE
QoS QUEUE

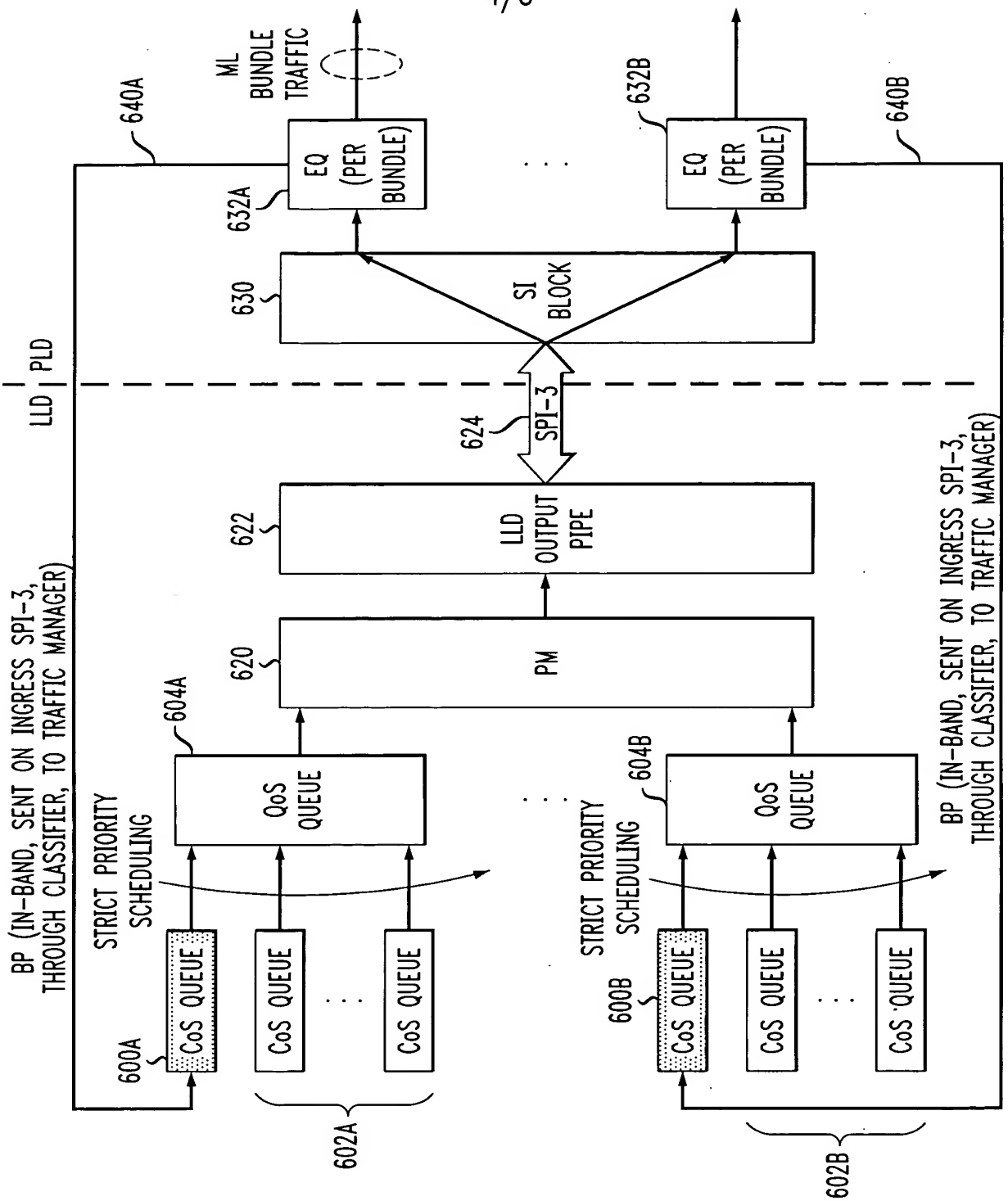

ML BUNDLE TRAFFIC
640A
632A
EQ (PER BUNDLE)
632B
640B
630
SI BLOCK
LLD
PLD
624
SPI-3
622
LLD OUTPUT PIPE
620
PM
604A
604B
QoS QUEUE
STRICT PRIORITY SCHEDULING
BP (IN-BAND, SENT ON INGRESS SPI-3, THROUGH CLASSIFIER, TO TRAFFIC MANAGER)
600A
600B
CoS QUEUE
602A
602B
ML TRAFFIC FOR SINGLE ML BUNDLE (QoS Q PER BUNDLE WITH OPTIONAL CoS Q PER DATA CLASS) xN ML BUNDLES
PPP OR GENERIC PACKET TRAFFIC FOR SINGLE HDLC CHANNEL (QoS Q PER BUNDLE WITH OPTIONAL CoS Q PER DATA CLASS) xN HDLC CHANNELS

FIG. 6

FIG. 7

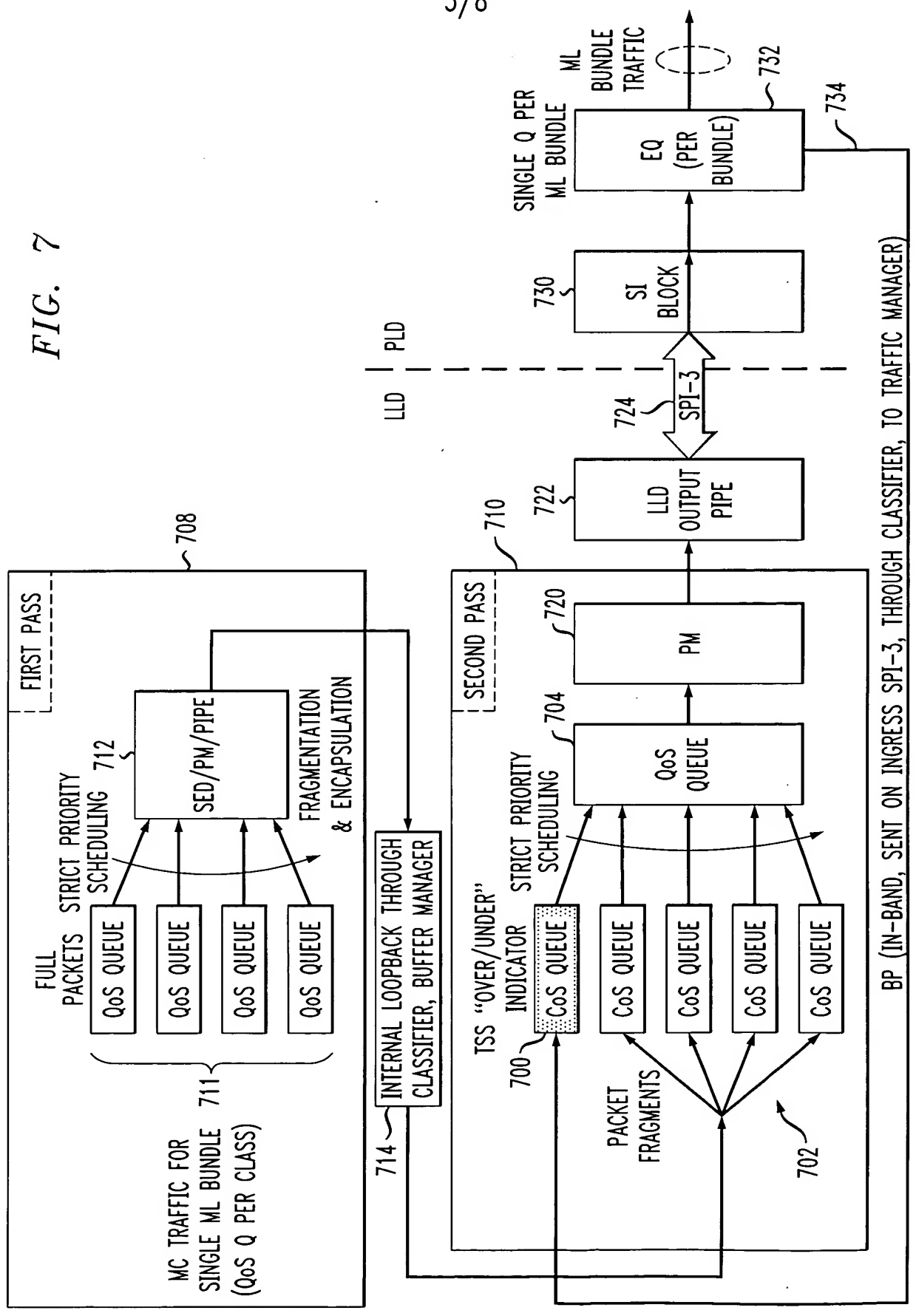

FIRST PASS
708
MC TRAFFIC FOR SINGLE ML BUNDLE (QoS Q PER CLASS)
711
FULL PACKETS
STRICT PRIORITY SCHEDULING
712
QoS QUEUE
QoS QUEUE
QoS QUEUE
QoS QUEUE
SED/PM/PIPE
FRAGMENTATION & ENCAPSULATION
714
INTERNAL LOOPBACK THROUGH CLASSIFIER, BUFFER MANAGER
SECOND PASS
710
TSS "OVER/UNDER" INDICATOR
700
STRICT PRIORITY SCHEDULING
704
CoS QUEUE
CoS QUEUE
CoS QUEUE
CoS QUEUE
CoS QUEUE
QoS QUEUE
PACKET FRAGMENTS
702
720
PM
722
LLD OUTPUT PIPE
724
SPI-3
LLD
PLD
730
SI BLOCK
SINGLE Q PER ML BUNDLE
EQ (PER BUNDLE)
732
ML BUNDLE TRAFFIC
734
BP (IN-BAND, SENT ON INGRESS SPI-3, THROUGH CLASSIFIER, TO TRAFFIC MANAGER)

FIG. 8

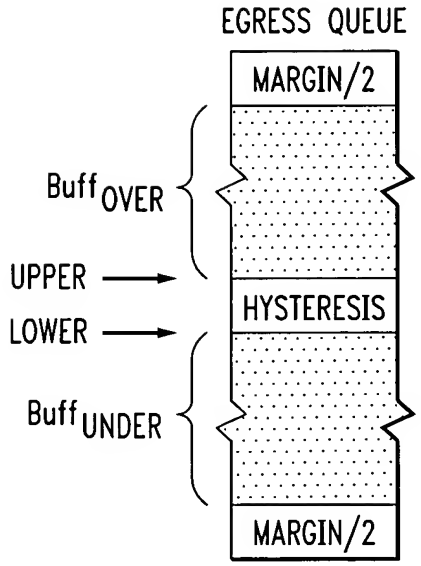

EGRESS QUEUE
MARGIN/2
Buff OVER
UPPER
HYSTERESIS
LOWER
Buff UNDER
MARGIN/2

FIG. 9

PARAMETER DEFINITIONS	
R_{PORT} : NOMINAL DATA RATE OF A PLD HDLC CHANNEL CORRESPONDING TO AN EQ.	D_{MTU} : DELAY DUE TO TRANSMISSION OF AN MTU-SIZED PACKET FROM LLD CoS QUEUE.
R_{FILL} : DATA INPUT (ENQUEUE) RATE OF PLD EQ.	D_{LLD} : WORST-CASE CLASSIFICATION DELAY OF LLD.
R_{DRAIN} : DATA OUTPUT (DEQUEUE) RATE OF PLD EQ.	D_{PIPE} : OUTPUT PIPELINE DELAY OF LLD.
FCL : FLOW CONTROL LATENCY.	D_{PLD} : PLD DELAY IN TRANSMITTING IBFC MESSAGE.

$$Buff = |R_{FILL} - R_{DRAIN}| * FCL$$

$$|R_{FILL} - R_{DRAIN}| = |R_{PORT} - 0.8\ R_{PORT}| = 0.2 * R_{PORT}\ ^{\dagger}$$

$$FCL = D_{MTU} + D_{LLD} + D_{PIPE} + D_{PLD}\ ^{\ddagger}$$

USE THE FOLLOWING FACTS AND WORST-CASE ASSUMPTIONS:

$$D_{MTU-L} = MTU \div (0.8 * R_{PORT});\ D_{MTU-U} = MTU \div R_{PORT}$$

$$D_{LLD} \leq 20\ \mu sec.^{\dagger\dagger}$$

$$D_{PIPE} \leq 6\ \mu sec.^{\ddagger\ddagger}$$

$$D_{PLD} \leq 1\ \mu sec.^{\S}$$

$$\begin{aligned} Buff_{UNDER} &= (0.2 * R_{PORT}) * ([MTU/(0.8 * R_{PORT})] + 20\ \mu s + 6\ \mu s + 1\ \mu s) \\ &= (0.2 * R_{PORT}) * ([MTU/(0.8 * R_{PORT})] + 27\ \mu s) \\ &= R_{PORT} * ([0.25 * MTU/R_{PORT})] + 5.4\ \mu s) \\ &= (0.25 * MTU) + (R_{PORT} * 5.4\ \mu s) \end{aligned}$$

$$\begin{aligned} Buff_{OVER} &= (0.2 * R_{PORT}) * ([MTU/R_{PORT}] + 20\ \mu s + 6\ \mu s + 1\ \mu s) \\ &= (0.2 * R_{PORT}) * ([MTU/R_{PORT}] + 27\ \mu s) \\ &= R_{PORT} * ([0.2 * MTU/R_{PORT})] + 6.75\ \mu s) \\ &= (0.2 * MTU) + (R_{PORT} * 6.75\ \mu s) \end{aligned}$$

†HDLC R_{DRAIN} IS AT MOST 20% GREATER OR LESS THAN SCHEDULER R_{FILL}

‡FCL IS EQUAL TO THE SUM OF THE DELAYS (D) SHOWN

††W.C. DELAY OF THE FLOW CONTROL MESSAGE THROUGH CLASSIFICATION TO THE TRAFFIC SHAPER

‡‡LLD OUTPUT PIPELINE DELAY

§W.C. DELAY FROM FLOW CONTROL MESSAGE GENERATION IN PLD TO TRANSMISSION ON THE SPI-3 INGRESS INTERFACE

FIG. 10

HDLC CHANNEL SIZE	HDLC CHANNEL RATE (IN Kbps)	MTU (IN BYTES)	$Buff_{UNDER}$ (IN BYTES)	$Buff_{OVER}$ (IN BYTES)	LOWER BOUND EQ SIZE (IN BYTES)	WORST-CASE EQ SIZE (IN BYTES)
DS0	64	576	145	116	261	586
	64	1518	380	304	684	1432
	64	9600	2401	1921	4322	8708
DS1	1544	576	146	117	263	590
	1544	1518	381	305	686	1436
	1544	9600	2402	1922	4324	8712
8 x DS1	12352	576	153	126	279	622
	12352	1518	388	315	703	1470
	12352	9600	2409	1931	4340	8744